AMENDMENT TO THE CLAIMS

1. (Previously Presented) A method for detecting and decoding data comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals to use as a factor for decoding said data;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to said known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

2. (Original) The method as described in claim 1, wherein said set of data signal received is a data packet that is in a serial data format, over a network line.

3. (Previously Presented) The method as described in claim 2, further comprising detecting said size of said received set of data signal and decoding said received set of data signals, detecting and decoding said size of said received set of data signal comprising:

converting a serial data packet into a parallel data format;

extracting a word clock from a received data packet;

incrementing a number held by a counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

4. (Previously Presented) The method as described in claim 3, wherein said act of extracting said destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated.

5. (Previously Presented) The method as described in claim 3, wherein said method of comparing said destination address to a known data value further comprises:

performing a comparison function upon said converted parallel set of data signals and said set of data from said memory circuitry;

generating a digital comparator status signal in response of said performance of comparator function; and

clocking in said digital comparator data signal into a register.

6. (Previously Presented) The method as described in claim 5, wherein said method of determining whether said received data signals should be received by said host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry.

7. (Original) The method as described in claim 6, wherein said output of said comparators are not latched when a mask circuitry indicates that a particular frame of data is not compared.

8. (Original) The method as described in claim 5, wherein said method of generating a status signal alerting said host circuitry further comprises performing an OR function upon all said latched output of said comparators.

9. (Previously Presented) The method as described in claim 1, wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host circuitry that a address match has been found.

10. (Previously Presented) An apparatus for detecting and decoding data, comprising:

means for receiving a data signal;

means for detecting a size of said received data signal;

a data formatter;

a clock divider;

a counter;

a host circuitry interface capable of transmitting and receiving data from a host circuitry, said host circuitry enter a wake up state from a sleep mode based upon decoded address data received by said host circuitry, said decoded address data being based_upon a content of_said data signal and said size of said received data signals;

a memory circuitry;

a plurality of comparators;

a mask circuitry;

a digital logic circuitry;

a plurality of status registers; and

a plurality of clocked registers.

11. (Original) The apparatus as described in claim 10, wherein said data formatter comprises of a serial to parallel converter and a data end detector that are capable of converting a serial stream of data into parallel data words and detecting an end of a data stream.

12. (Original) The apparatus as described in claim 10, wherein said clock divider is capable of incrementing a count held by said counter.

13. (Original) The apparatus as described in claim 10, wherein said memory circuitry comprises of a memory element and a memory data access logic.

14. (Original) The apparatus as described in claim 13, wherein said memory element is coupled with said memory data access logic such that data from said memory element can be retrieved and sent through said memory data access logic.

15. (Original) The apparatus as described in claim 14, wherein said memory data access logic is coupled with said host interface such that data can be sent to and retrieved from said memory elements.

16. (Original) The apparatus as described in claim 10, wherein said comparators are coupled with said data formatter such that said comparators receive parallel formatted data from said data formatter.

17. (Original) The apparatus as described in claim 16, wherein said comparators are further coupled with said memory circuitry such that said comparator is capable of receiving data from said memory circuitry.

18. (Original) The apparatus as described in claim 17, wherein at least one output from said comparators is further coupled to said digital logic circuitry and said clock registers such that said output of said comparators is latched by said digital logic circuitry and said clock registers.

19. (Original) The apparatus as described in claim 18, wherein said mask circuitry is capable of preventing a registering of said comparator output into said clocked registers.

20. (Original) The apparatus as described in claim 18, wherein said status registers are coupled to said digital logic circuitry and said clocked registers such that said latched comparator outputs are inputted into said status registers.

21. (Original) The apparatus as described in claim 10, wherein an output from said digital logic circuitry is clock-registered by a signal output from said data formatter.

22. (Previously Presented) The apparatus as described in claim 10, wherein said status registers are coupled with said host interface such that data from said status register could be retrieved through an access port.

23. (Previously Presented) A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method, comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals to use as a factor for decoding said data signals;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to said known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

24. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said set of data signal received is a data packet that is in a serial data format, over a network line.

25. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 24, further comprising detecting said size of said received set of data signal and decoding said received set of data signals, detecting and decoding said size of said received set of data signal comprising:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

26. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said act of extracting said destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated.

27. (Previously Presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said method of comparing said destination address to said known data value further comprises:

performing a comparison function upon said converted, parallel set of data signals, and said set of data from said memory circuitry;

generating a digital comparator status signal in response of said performance of comparator function; and

clocking in said digital comparator data signal into a register.